IN THE UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of

Devins et al.

Serial No.: 10/060,750 Group Art Unit: 2123

Filed: January 30, 2002 Examiner: Russell L. Guill

For: SYSTEM FOR CONTROLLING EXTERNAL MODELS USED FOR VERIFICATION OF SYSTEM IN A CHIP (SOC) INTERFACES

Honorable Commissioner of Patents
Alexandria, Virginia 22313-1450

APPELLANTS' BRIEF ON APPEAL UNDER 35 U.S.C. §134(a)

Sir:

Appellants respectfully appeal the decision of the Examiner in the final rejection of claims 2 and 8-27 in the Final Office Action mailed December 17, 2008.

I. STATEMENT OF THE REAL PARTY OF INTEREST

The real party of interest is IBM Corporation, assignee of 100% interest of the above-referenced patent application.

II. STATEMENT OF RELATED CASES

There are no other appeals or interferences known to Appellants, Appellants'

legal representative or Assignee, which would directly affect or be directly affected by or have a bearing on the Board's decision on this appeal.

III. JURISDICTIONAL STATEMENT

The Board has jurisdiction under 35 U.S.C. 134(a). The Examiner mailed a Final Rejection on December 17, 2008 setting a three-month shortened statutory period for response. The time for responding to the Final Rejection expired on March 17, 2009. Rule 134. A Notice of Appeal was filed on March 16, 2009. The time for filing an Appeal Brief is two months after the filing of a Notice of Appeal. Bd.R. 41.37(c). The time for filing an Appeal Brief expired on May 16, 2009 (being a Federal holiday). The Appeal Brief is being filed on May 12, 2009; therefore, this Appeal Brief is proper and is filed timely.

IV. TABLE OF CONTENTS

V. TABLE OF AUTHORITIES

Not applicable.

VI. STATUS OF AMENDMENTS

An Amendment, filed October 17, 2008, was entered by the Examiner.

VII. GROUNDS OF REJECTION TO BE REVIEWED

Claims 2 and 8-27 are rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

Claims 2 and 8-27 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

Claims 2, 8-14, and 15-20 are rejected under 35 U.S.C. §101 because the claimed invention is directed to non-statutory subject matter.

VIII. STATEMENT OF FACTS

[0001] It is a fact that the 'Description of Related Art' section of the present invention discloses, "Hardware verification typically entails the use of software "models" of design logic. Such models may be implemented as a set of instructions in a hardware description language (HDL)." (Specification, paragraph [0003]).

[0002] It is a fact that the 'Description of Related Art' section of the present invention discloses, "The term "SOC" as used herein refers to combinations of discrete logic blocks, often referred to as "cores," each performing a different function or group of functions. A SOC integrates a plurality of cores into a single silicon device, thereby providing a wide range of functions in a highly compact form." (Specification, paragraph [0004]).

[0003] It is a fact that the 'Description of Related Art' section of the present invention discloses, "In its developmental stages, a core is typically embodied as a simulatable HDL model written at some level of abstraction, or in a mixture of abstraction levels. ... A core may be in the form of a netlist including structural and logic gate elements or a behavioral model." (Specification, paragraph [0005]).

[0004] It is a fact that the 'Description of Related Art' section of the present invention discloses, "Verification of a SOC presents challenges because of the

number of cores and the complexity of interactions involved, both between the cores internally to the SOC, and between the SOC and external logic." (Specification, paragraph [0006]).

[0005] It is a fact that the 'Description of Related Art' section of the present invention discloses, "According to one standard technique, already-verified models are used to test other models. The electronic design automation (EDA) industry has reached a level of sophistication wherein vendors offer standardized models for use in verification of other models still in development. In particular, such models are typically used for testing cores in a SOC that have external interfaces (i.e., communicate with logic external to the SOC)." (Specification, paragraph [0007]).

[0006] It is a fact that the 'Description of Related Art' section of the present invention discloses, "However, there are disadvantages associated with using standardized models." (Specification, paragraph [0008]).

[0007] It is a fact that the 'SUMMARY OF THE INVENTION' section of the present invention discloses, "In view of the foregoing and other problems, disadvantages, and drawbacks of the conventional verification test benches, the present invention has been devised, and it is an object of the present invention to provide a structure that attaches an external model to a SOC interface and to an

external bus interface unit." (Specification, paragraph [0010]).

[0008] It is a fact that the 'DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION' section of the present invention discloses, "The invention provides a structure that controls an external model(s) used for interconnection verification of an SOC interface. An important feature of the invention is to connect the external model to an external bus interface unit (EBIU) via a local bus. The EBIU is then connected to the SOC's EBIU. This connection enables the external model to be completely controlled from the test case running in the SOC by using the EBIU's external bus mastering capability. The EBIU in this invention is not a specific core or unit and is meant to refer to any communications channel that can connect the SOC to the external model and provide the external bus mastering functionality. This allows the test case to program the external model to perform such tasks as data transfers and other interface specific functions necessary to thoroughly verify the SOC interface. The same test case is also used to program the SOC interface." (Specification, paragraph [0018]).

[0009] It is a fact that the 'DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION' section of the present invention

discloses, "... the present invention implements control by attaching an EBIU 200 to an external interface model 210 (e.g., a verification interface model) via a local bus structure 201, as shown in Figure 1. This essentially creates enough of an external SOC structure 300 (e.g., a verification test bench) that is capable of having data or commands transferred from an external source (the SOC 100 in this case) through the test bench EBIU 200 into or through the verification interface model 210." (Specification, paragraph [0019]).

[0010] It is a fact that FIG. 1 of the present invention discloses,

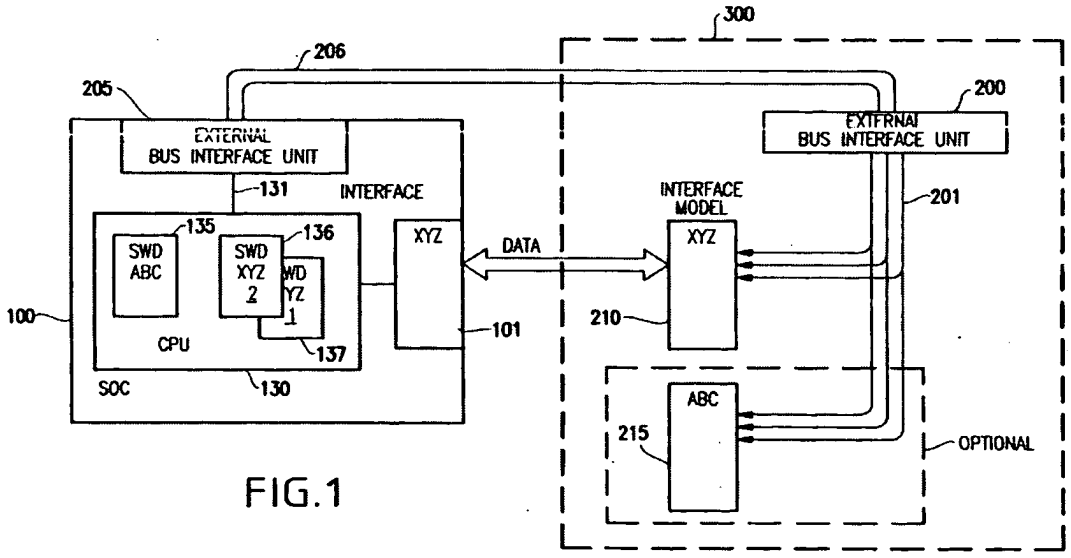

FIG.1

[0011] It is a fact that the 'DETAILED DESCRIPTION OF PREFERRED

EMBODIMENTS OF THE INVENTION' section of the present invention discloses, "The test bench EBIU 200 attaches to the SOC EBIU 205 via an external bus 206. The internal bus structure 201 within the verification test bench 300 is implemented to respond to an address range that is unique to the SOC, giving complete control to a single verification test running in the SOC 100. In addition, Figure 1 illustrates various internal components of the SOC 100 including the central processing unit (CPU) 130 and the test patterns 135-137." (Specification, paragraph [0020]).

[0012] It is a fact that the 'DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION' section of the present invention discloses, "In operation, the structure in Figure 1 utilizes the interface model 210 to test the SOC's interface 101. A bus master can configure other units or cores connected to a bus, whereas a bus slave can only respond to a master's commands. The EBIU 200 (slave) responds to external bus master commands from the CPU 130, thereby enabling a test case running in the SOC 100 to direct the CPU 130 (which is a master on the SOC's internal bus 131) to act as a master on the test bench's internal bus 201. Thus, the test case running in the SOC 100 can direct the SOC CPU 130 to program (e.g., master) the registers in both the internal interface

101 and the interface model 210. Here the same test case software is used to program both the SOC's interface 101 and the external entity's 300 interface model 210." (Specification, paragraph [0022]).

[0013] It is a fact that the 'DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION' section of the present invention discloses, "In Figure 1, the invention transfers data from the external interface model 210 to the SOC interface 101. The test case calls the software driver (SWD) 135-137 for the interface 101 and instructs the software driver to configure the interface 101 to receive data. Next, the test case calls the same SWD 135-137 and instructs the software driver to configure the external interface model 210 to send data. The SOC's interface 101 and the external interface model 210 are implemented to respond to different unique addresses. Thus, when the test case calls the SWD 135-137 to perform some configuration on one of the interfaces, the test case sends the address of that interface along with the operation to be performed. The test case then sends test data to the unique data address of the external interface model 210. This data is sent from the SOC 100 through the SOC's external bus interface unit (EBIU) 205 to the external EBIU 200 and then along to the interface model 210. From there the data is sent through the interface model 210

into the SOC's interface 101 which is configured to receive data. Once the data is back in the SOC 100, the test case checks it for correctness and a test status is recorded." (Specification, paragraph [0023]).

[0014] It is a fact that the 'DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION' section of the present invention discloses, "One advantage achieved with the invention is better software control. The invention allows the test case executing in the SOC 100 to use the same software driver, if appropriate, to program both interfaces 101, 210. The test case can also use one driver to program the SOC interface 101 and another to program the interface model 210, both of which are controlled by the test case. This is an improvement over the conventional situation where the test case running within the SOC 100 controls the SOC interface 101, and another software program (written in a bus functional language) controls the external interface 210. The invention provides increased reusability and decreased development time because the invention uses the same or similar software written in the same language to program both interfaces." (Specification, paragraph [0024]).

[0015] It is a fact that the 'DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION' section of the present invention

discloses, "Figure 2 shows a computer system which can be used to implement the present invention. The system includes a computer 400 comprising a memory 401 and processor 402 which may be embodied, for example, in a workstation. The system may include a user interface 403 comprising a display device 404 and user input devices such as a keyboard 405 and mouse 406. The verification test bench 450 may be implemented as computer-executable instructions which may be stored on computer-usable media such as disk storage 407, CD-ROM 408, magnetic tape 409 or diskette 410. The instructions may be read from a computer-usable medium as noted into the memory 401 and executed by the processor 402 to effect the advantageous features of the invention. A simulator 411 loaded into computer memory 401 and executed by processor 402 interprets a compiled verification test bench to simulate hardware devices corresponding thereto. The simulator 411 may be any of a variety of commercially available simulators, including event simulators, cycle simulators and instruction set simulators. Programming structures and functionality implemented in computer-executable instructions as disclosed herein-above for performing steps of the method may find specific implementations in a variety of forms, which are considered to be within the abilities of a programmer of ordinary skill in the art." (Pub. No. 2003/0145290, paragraph

[0027]).

[0016] It is a fact that FIG. 2 of the present invention discloses,

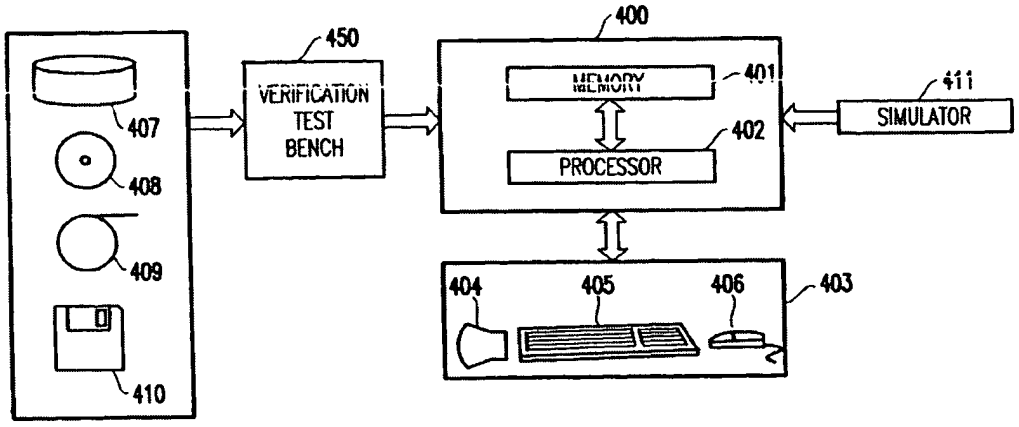

FIG.2

IX. ARGUMENT

A. The rejection of claims 2 and 8-27 under 35 U.S.C. §112, first paragraph.

1. Appellants' argument with respect to Independent Claims 2, 8, 15, and 21.

[0017] In the Final Office Action, the Examiner argues the rejection of independent claims 2, 8, and 15, and their dependent claims, in the following three paragraphs.

[0018] The Final Office Action states, " Regarding claim 2 and dependent claims: claim 2 recites a CPU, an SOC interface and EBIU interfaces that the Applicant has argued as being physical hardware; however! the specification appears to be directed to software models of a CPU, an SOC interface and EBIU interfaces that are implen1ented in a computer system (see especially paragraph [0025] "Figure 2 shows a computer system which can be used to implement the present invention"! and paragraphs [0001] -[0008]). The specification appears to be directed to verification of HDL models of a SOC (see especially paragraphs {0001]-- {0008]), and does not appear to intend to support a system with a physical CPU/ a physical SOC interface; and physical EBIU interfaces. Especially see the specification paragraphs [0004]-- [0005] that appear to define an SOC as cores, and

a core is embodied as a simulatable HDL model, and may be in the form of a netlist." (Final Office Action, mailed 12/17/2008, page 13, section 6.a.).

[0019] The Final Office Action states, " Regarding claim 8 and dependent claims: claim 8 recites a CPU; an SOC interface and EBIU interfaces that the Applicant has argued as being physical hardware. The specification appears to be directed to software models of a CPU, an SOC interface and EBIU interfaces that are implemented in a computer system (see especially paragraph [0025]; "Figure 2 shows a computer system which can be used to implement the present invention" and paragraphs [0001] ... [0008]). The specification appears to be directed to verification of HDL models of a SOC (see especially paragraphs [0001] - [0008] and does not appear to intend to support a system with a physical CPU, a physical SOC interface! and physical EBIU interfaces. Especially see the specification paragraphs [0004] - [0005] that appear to define an SOC as cores and a core is embodied as a simulatable HDL model; and may be in the form of a netlist." (Final Office Action, mailed 12/17/2008, page 13, section 6.b.).

[0020] The Final Office Action states, "Regarding claim 15 and dependent claims: claim 15 recites a CPU/ an SOC interface and EBIU interfaces that the Applicant has argued as being physical hardware. The specification appears to be

directed to software models of a CPU, an SOC interface and EBIU interfaces that are implemented in a computer system (see especially paragraph [0025]; "Figure 2 shows a computer system which can be used to implement the present invent-ion"! and paragraphs [0001] - [0008]). The specification appears to be directed to verification of HDL models of a SOC (see especially paragraphs [0001]- [O008]), and does not appear to intend to support a system with a physical CPU a physical SOC interface! and physical EBIU interfaces. Especially see the specification paragraphs [0004] - [0005] that appear to define an SOC as cores and a core is embodied as a simulatable HDL model; and maybe in the form of a netlist." (Final Office Action, mailed 12/17/2008, page 13, section 6.c.).

[0021] The Final Action did not provide arguments for the rejection of independent claim 21 and its dependent claims under 35 U.S.C. §112, first paragraph; however, Appellants have assumed that the argument for rejection of independent claim 21 and its dependent claims is similar to those arguments for the rejection of independent claims 2, 8, and 15, and their dependent claims.

[0022] In the Final Office Action's rejection of the claims under 35 U.S.C. §112, first paragraph, immediately above, the Examiner cites paragraphs [0001]-[0008] and [0025] of the originally filed Specification and Figure 2. As argued

previously, Appellants respectfully point out that that paragraphs [0002]-[0008] describe the 'Description of Related Art' section of the Specification (Amendment, filed 02/17/2009, paragraphs [0003] and [0005]), while paragraph [0001] describes the "Field of the Invention' section of the Specification. (emphases added). (Amendment, filed 02/17/2009, paragraph [0005]).

[0023] As previously argued, Appellants respectfully assert that paragraph [0025] and Figure 2, cited by the Examiner in his rejection, describe an embodiment of the invention, which is not claimed by the present application. (Amendment, filed 02/17/2009, paragraph [0009]).

[0024] However, as argued previously, Appellants respectfully assert that the claimed invention is disclosed by paragraphs [0019]-[0024] of the originally filed Specification in the 'DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION' section of the Specification and Figure 1. (Amendment, filed 02/17/2009, paragraph [0012]).

[0025] Therefore, as previously argued, Appellants respectfully argue that paragraphs [0002]-[0008], cited by the Examiner in his rejection, describe the Related Art, and not the present invention, which is disclosed in paragraphs [0019]-[0024] and Figure 1. (Amendment, filed 02/17/2009, paragraphs [0011] and

[0012]).

[0026] Furthermore, as argued previously, Appellants assert that the Examiner has misconstrued the plain meaning of paragraphs [0002]-[0009] of the 'Description of the Related Art' section of the Specification as it relates to the 'Related Art.' Appellants respectfully assert that to one of ordinary skill in the art, paragraphs [0002]-[0009] may be paraphrased as follows: Hardware verification of integrated circuits typically entails use of software models for logic blocks. A system-on-a chip (SOC) comprises a number of logic blocks, also called "cores", which are integrated into a single silicon device. Conventional techniques of verification of the logic blocks of an SOC may use HDL models or netlists. However, hardware verification of an SOC presents challenges because of the complexity of interaction between logic blocks of the SOC and between the SOC and external logic devices. Standardized software models used for models of the logic blocks, still in development, have disadvantages. (Amendment, filed 02/17/2009, paragraph [0005]).

[0027] In other words and as argued previously, according to the 'Description of the Related Art' section of the Specification, hardware verification by software

models of the logic blocks, comprising an SOC, has disadvantages. (Amendment, filed 02/17/2009, paragraph [0006]).

[0028] Therefore, as recited in paragraph [0010] of the Specification in the SUMMARY OF THE INVENTION section, "In view of the foregoing and other problems, disadvantages, and drawbacks of the conventional verification test benches, the present invention has been devised, and it is an object of the present invention to provide a structure [i.e., hardware] that attaches an external model to a SOC interface [i.e., hardware] and to an external bus interface unit [i.e., hardware]." (Specification, paragraph [0010]).

[0029] As is known to those in the art of chip design and verification, verification by software has its disadvantages. In particular, race conditions are difficult to resolve through software verification. For example, imagine a 2-input NAND gate within a chip to be verified. The first input to the NAND gate derives from a logic block comprising 10 gates, whereas the second input to the NAND gate derives from a logic block comprising 15 gates. The first input signal will arrive at the NAND before the second input (assuming length and impedances of the input lines are approximately equal). That is, the proper output for the NAND gate is not when the first input arrives but is delayed by the timing of the second

input, and whatever delays there are associated with the NAND gate itself. In the floor planning of a hardware SOC, delays within and between logic blocks (even when CLOCKed) can lead to errors from expected functional outputs. Thus, the present invention uses a hardware SOC to test itself, by running test patterns on itself, sending the results to an external verification test bench that includes a verification interface model, which also receives signals from a hardware SOC interface, to verify the hardware logic of the hardware SOC.

[0030] The Final Action states, "Claims 2 and 8-27 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(c) contains subject matter which is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention." (Final Office Action, mailed 12/17/2009, page 13, section 6.).

[0031] As disclosed by paragraphs [0019], [0020], and [0022]-[0024] of the Specification, provided in the 'Statement of Fact's section of the Appeal Brief, above, and as shown in Figure 1 of the present invention below,

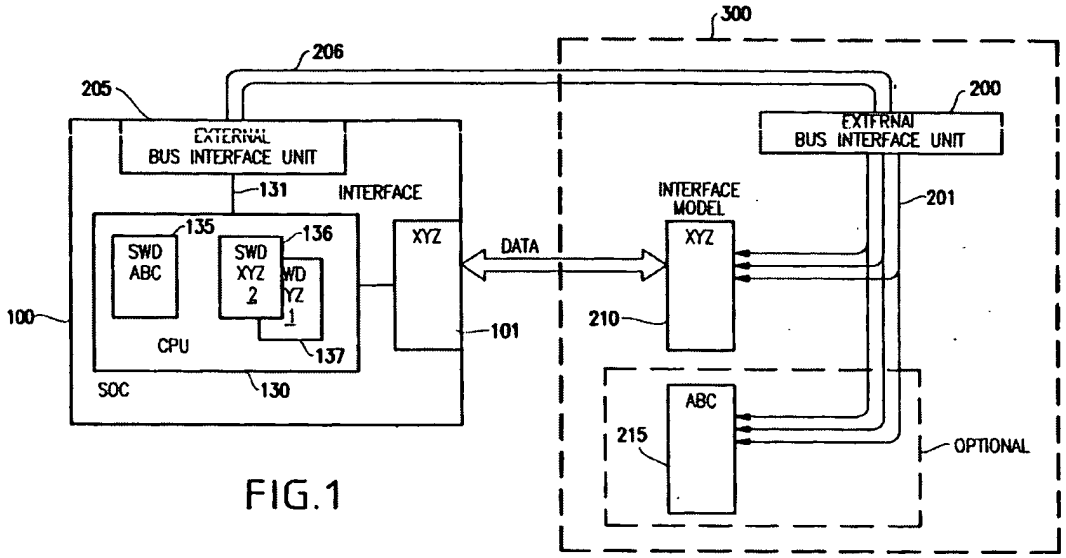

FIG.1

Appellants respectfully submit that the written description describes at least the features of: a system-on-a-chip (SOC), 100; an SOC interface, 101; a central processing unit (CPU), 130; an internal SOC bus, 131; test patterns/software drivers 135-137; a slave external bus interface unit, 200; test bench's internal bus, 201; a master external bus interface unit, 205; an external bus, 206; an external verification interface model, 210; and an optional extra external verification interface model, 215.

[0032] As disclosed by paragraphs [0019]-[0024] from the Specification, above, and as disclosed by the 'Appendix of Claims' of this Appeal Brief, which

supports through annotation the features defined by independent claims 2, 8, 15, and 21, Appellants respectfully argue that the written description reasonably conveys to one skilled in the relevant art that the inventors, at the time the invention was filed, had possession of the claimed invention.

[0033] For at least the reasons outlined above, Appellants respectfully submit that independent claims 2, 8, 15, and 21 fulfill the written description requirement of 35 U.S.C. §112, first paragraph. Withdrawal of the rejection of independent claims 2, 8, 15, and 21 under 35 U.S.C. §112, first paragraph, is respectfully solicited.

2. Appellants' argument with respect to Dependent Claims 9-14, 16-20, and 22-27.

[0034] As disclosed by paragraphs [0019]-[0024] from the Specification, above, and as disclosed by the 'Appendix of Claims' of this Appeal Brief, which supports through annotation the features defined by dependent claims 9-14, 16-20, and 22-27, Appellants respectfully argue that the written description reasonably conveys to one skilled in the relevant art that the inventors, at the time the invention was filed, had possession of the claimed invention.

[0035] For at least the reasons outlined above, Appellants respectfully submit that dependent claims 9-14, 16-20, and 22-27 fulfill the written description requirement of 35 U.S.C. §112, first paragraph. Withdrawal of the rejection of independent claims 9-14, 16-20, and 22-27 under 35 U.S.C. §112, first paragraph, is respectfully solicited.

B. The rejection of claims 2 and 8-27 under 35 U.S.C. §112, second paragraph.

1. Appellants' argument with respect to Independent Claims 2, 8, 15, and 21.

[0036] The Final Office Action states, "... the independent claims 2, 8 and 15 appear to be directed to a physical hardware system; however the specification appears to be directed to a software model of a physical hardware system *(Especially see the specification paragraphs [0004] - [0005] that appear to define an SOC as cores, and a core is embodied as a simulatable EDL model, and may be in the form of a netlist).* It is unclear whether the claims are directed to physical hardware or a software model. Any elements of the claims that are intended to be physical hardware should be clearly distinguished as physical hardware, and similarly, software elements should be distinguished." (Final Office Action, mailed 12/17/2009, page 15, section 7.a. i).

[0037] The Final Office Action states, "Regarding independent claims 21, and dependent claims: the independent claims appear to be directed to a method that uses physical hardware; however the specification appears to be directed to a software model of a physical hardware system *(Especially see the specification paragraphs [0004] .. [0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist).* It is unclear whether the claims are directed to a method that uses physical hardware or a software model. Any elements of the claims that are intended to be physical hardware should be clearly distinguished as physical hardware, and similarly, software elements should be distinguished." (Final Office Action, mailed 12/17/2009, page 15, section 7.a. ii).

[0038] As argued previously and above, Appellants respectfully point out that that paragraphs [0002]-[0008] describe the 'Description of Related Art' section of the Specification (Amendment, filed 02/17/2009, paragraphs [0003] and [0005]), while paragraph [0001] describes the "Field of the Invention' section of the Specification. (emphases added). (Amendment, filed 02/17/2009, paragraph [0005]).

[0039] As argued previously and above, Appellants respectfully assert that the claimed invention is disclosed by paragraphs [0019]-[0024] of the originally filed Specification in the 'DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION' section of the Specification and Figure 1. (Amendment, filed 02/17/2009, paragraph [0012]).

[0040] Therefore, as argued, previously and above, Appellants respectfully argue that paragraphs [0002]-[0008], cited by the Examiner in his rejection, describe the Related Art, and not the present invention, which is disclosed in paragraphs [0019]-[0024] and Figure 1. (Amendment, filed 02/17/2009, paragraphs [0011] and [0012]).

[0041] As disclosed by paragraphs [0019]-[0024] from the Specification, above, and as disclosed by the 'Appendix of Claims' of this Appeal Brief, which supports through annotation the features defined by independent claims 2, 8, 15, and 21, Appellants respectfully argue that independent claims 2, 8, 15, and 21 particularly point out and distinctly claim the subject matter which Appellants regard as the invention, and thus, fulfill the statutory requirements of 35 U.S.C. §112, second paragraph paragraph. Withdrawal of the rejection of independent

claims 2, 8, 15, and 21 under 35 U.S.C. §112, second paragraph, is respectfully solicited.

2. Appellants' argument with respect to Dependent Claims 9-14, 16-20, and 22-27.

[0042] As disclosed by paragraphs [0019]-[0024] from the Specification, above, and as disclosed by the 'Appendix of Claims' of this Appeal Brief, which supports through annotation the features defined by dependent claims 9-14, 16-20, and 22-27, Appellants respectfully argue that dependent claims 9-14, 16-20, and 22-27 particularly point out and distinctly claim the subject matter which Appellants regard as the invention, and thus, fulfill the statutory requirements of 35 U.S.C. §112, second paragraph. Withdrawal of the rejection of dependent claims 9-14, 16-20, and 22-27 under 35 U.S.C. §112, second paragraph, is respectfully solicited.

C. The rejection of claims 2, 8-14, and 15-20 under 35 U.S.C. §101.

1. Appellants' argument with respect to Independent Claims 2, 8, 15, and 21.

[0043] The Final Office Action states, "Regarding claims 21-27, the method is performed in a software environment inherently requiring a computer to perform the method, and thus is considered statutory because it is inherently tied to a

computer to perform the method." (Final Office Action, mailed 12/17/2009, page 16, section 9).

[0044] The Final Office Action states, "Regarding claims 2, 8 -14, 15- 20, the claims are directed to a system for verification of integrated circuit logic of a system-on-chip, but none of the claim limitations appear to expressly or inherently require tangible physical components *(Especially see the specification paragraphs [0004] - [0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist. Also especially paragraph [0025], "Figure 2 shows a computer system which can be used to implement the present invention," and paragraphs [0001] -[0008]).*" (Final Office Action, mailed 12/17/2009, page 17, section 10.a).

[0045] As argued previously and above, Appellants respectfully assert that paragraph [0025] and Figure 2, cited by the Examiner in his rejection, describe an embodiment of the invention, which is not claimed by the present application. (Amendment, filed 02/17/2009, paragraph [0009]).

[0046] As argued previously and above, Appellants respectfully point out that that paragraphs [0002]-[0008] describe the 'Description of Related Art' section of the Specification (Amendment, filed 02/17/2009, paragraphs [0003] and [0005]),

while paragraph [0001] describes the "Field of the Invention' section of the Specification. (emphases added). (Amendment, filed 02/17/2009, paragraph [0005]).

[0047] As argued previously and above, Appellants respectfully assert that the claimed invention is disclosed by paragraphs [0019]-[0024] of the originally filed Specification in the 'DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION' section of the Specification and Figure 1. (Amendment, filed 02/17/2009, paragraph [0012]).

[0048] Therefore, as argued, previously and above, Appellants respectfully argue that paragraphs [0002]-[0008], cited by the Examiner in his rejection, describe the Related Art, and not the present invention, which is disclosed in paragraphs [0019]-[0024] and Figure 1. (Amendment, filed 02/17/2009, paragraphs [0011] and [0012]).

[0049] As disclosed by paragraphs [0019]-[0024] from the Specification, above, and as disclosed by the 'Appendix of Claims' of this Appeal Brief, which supports through annotation the features defined by independent claims 2, 8, and 15, Appellants respectfully argue that independent claims 2, 8, and 15 describe tangible physical components of a system for verifying integrated circuit logic of a

system-on-a-chip (SOC) and that the method of independent claim 2 is also described in paragraphs [0019]-[0024] of the Specification. Therefore, Appellants respectfully submit that independent claims 2, 8, and 15 are directed to statutory subject matter under 35 U.S.C. §101. Withdrawal of the rejection of independent claims 2, 8, and 15 under 35 U.S.C. §101 is respectfully solicited.

2. Appellants' argument with respect to Dependent Claims 9-14 and 16-20.

[0050] As disclosed by paragraphs [0019]-[0024] from the Specification, above, and as disclosed by the 'Appendix of Claims' of this Appeal Brief, which supports through annotation the features defined by dependent claims 9-14 and 16-20 Appellants respectfully argue that dependent claims 9-14 and 16-20 describe tangible physical components of a system for verifying integrated circuit logic of a system-on-a-chip (SOC). Therefore, Appellants respectfully submit that dependent claims 9-14 and 16-20 are directed to statutory subject matter under 35 U.S.C. §101. Withdrawal of the rejection of dependent claims 9-14 and 16-20 under 35 U.S.C. §101 is respectfully solicited.

IX. CONCLUSION

In view of the foregoing, Appellants submit that claims 2 and 8-27, all of the claims presently pending in the application, are in condition for allowance. Thus, the Board is respectfully requested to remove the rejections of claims 2 and 8-27.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 09-0456.

Respectfully Submitted,

Date: May 7, 2009

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APPENDIX

CLAIMS SECTION

1. (Canceled).

2. (Rejected) A system for verifying integrated circuit logic of a system-on-a-chip (SOC), said system comprising:

an SOC comprising:

a master central processing unit (CPU) that produces a first set of signals and a second set of signals for verifying said integrated circuit logic in response to running a verification case;

an SOC interface that receives said second set of signals; and

a first external bus interface unit (EBIU) that is slaved to said master CPU and receives said first set of signals; and

a verification test bench that is external to said SOC, said verification test bench comprising:

a verification interface model connected to said SOC interface; and

a second EBIU connected to said first EBIU and to said verification interface model;

wherein said first set of signals received by said second EBIU is inputted to said verification interface model and said verification interface model outputs data for said verification case to said SOC interface; and

wherein said verification case checks for correctness of said outputted data from said verification interface model to said SOC interface by said second set of signals and records a verification case status.

3-7. (Canceled).

8. (Rejected) A system for verifying integrated circuit logic of a system-on-a-chip (SOC), said system comprising:

an SOC comprising:

a master central processing unit (CPU) that produces a first set of signals and a second set of signals for verifying said integrated circuit logic in response to signals produced by running a verification case;

an SOC interface that receives said second set of signals, said SOC interface being connected to said master CPU by a first internal bus; and

a first external bus interface unit (EBIU) that is slaved and connected

to said master CPU by a second internal bus; and

a verification test bench that is external to said SOC, said verification test bench comprising:

a verification interface model connected to said SOC interface by a second external bus; and

a second EBIU connected to said first EBIU by a first external bus and to said verification interface model by a third internal bus;

wherein said first set of signals received by said second EBIU is inputted to said verification interface model via said third internal bus and said verification interface model outputs data for said verification case to said SOC interface via said data bus; and

wherein said verification case checks for correctness of said outputted data from said verification interface model to said SOC interface by said second set of signals via said first internal bus and records a verification case status.

9. (Rejected) The system in claim 8, wherein said verification case comprises software drivers.

10. (Rejected) The system in claim 8, wherein registers of said SOC interface and said verification interface model are controlled by the same verification case.

11. (Rejected) The system in claim 10, wherein said verification case utilizes the same software driver to configure and control said SOC interface and said verification interface model.

12. (Rejected) The system in claim 10, wherein said verification case utilizes different software drivers to configure and control said SOC interface and said verification interface model.

13. (Rejected) The system in claim 8, wherein said verification interface model tests an operational capability of said SOC interface.

14. (Rejected) The system in claim 8, further comprising an additional verification interface model for said verification test bench, said additional verification interface model being connected to said second EBIU for testing additional types of SOC interfaces.

15. (Rejected) A system for verifying integrated circuit logic of a system-on-a-chip (SOC), said system comprising:

an SOC comprising:

a master central processing unit (CPU) that produces a first set of signals and a second set of signals for verifying said integrated circuit logic in response to signals produced by running a verification case;

an SOC interface that receives said second set of signals, said SOC interface being connected to said master CPU by a first internal bus; and

a first external bus interface unit (EBIU) that is slaved and connected to said master CPU by a second internal bus; and

a verification test bench that is external to said SOC, said verification test bench comprising:

a verification interface model connected to said SOC interface by a second external bus; and

a second EBIU connected to said first EBIU by a first external bus and to said verification interface model by a third internal bus;

wherein said second EBIU and said first EBIU are mastered by

said master CPU of said SOC, such that, said SOC interface and said verification interface model receive said first set of signals and said second set of signals, respectively, as inputs based on the running of said verification case by said master CPU; and

wherein said verification case checks for correctness of outputted data from said verification interface model to said SOC interface by said second set of signals and records a verification status.

16. (Rejected) The system in claim 15, wherein said verification case comprises software drivers.

17. (Rejected) The system in claim 15, wherein said verification case utilizes the same software driver to configure and control said SOC interface and said verification interface model.

18. (Rejected) The system in claim 15, wherein verification test case utilizes different software drivers to configure and control said SOC interface and said verification interface model.

19. (Rejected) The system in claim 15, wherein said verification interface model tests an operational capability of said SOC interface.

20. (Rejected) The system in claim 15, further comprising an additional verification interface model for said verification test bench, said additional verification interface model being connected to said second EBIU for testing additional types of SOC interfaces.

21. (Rejected) A method for verifying integrated circuit logic of a system-on-a-chip (SOC), said method comprising:

producing a first set of signals and a second set of signals by a master central processing unit (CPU) of an SOC, which includes said integrated circuit logic, in response to running a verification case on said master CPU;

slaving an SOC interface, which receives said second set of signals, and a first external bus interface unit (EBIU) of said SOC, which receives said first set of signals, to said master CPU of said SOC;

connecting said SOC interface to an external verification interface model,

which is external to said SOC;

connecting said first EBIU to a second EBIU, which is external to said SOC, said second EBIU being connected to said external verification interface model;

inputting said first set of signals, received by said second EBIU, into said verification interface model;

inputting said second set of signals, received by said SOC interface; and

verifying said verification case by checking for correctness of said outputted data from said verification interface model to said SOC interface by said second set of signals and recording a verification case status.

22. (Rejected) The method in claim 21, wherein said verification case comprises software drivers.

23. (Rejected) The method in claim 21, further comprising controlling registers of said SOC interface and said verification interface model by the running of the verification case on the master CPU.

24. (Rejected) The method in claim 23, wherein said verification case utilizes the

same software driver to configure and control said SOC interface and said verification interface model.

25. (Rejected) The method in claim 23, wherein said verification case utilizes different software drivers to configure and control said SOC interface and said verification interface model.

26. (Rejected) The method in claim 21, further comprising comparing said first set of signals, received by said second EBIU, and inputted into said verification interface model and said second set of signals, received from said SOC interface, and inputted into said verification interface model to test an operational capability of said SOC interface.

27. (Rejected) The method in claim 21, further comprising:

connecting at least one additional verification interface model to said second EBIU; and

testing additional types of SOC interfaces.

28-34. (Canceled).

APPENDIX

CLAIM SUPPORT AND DRAWING ANALYSIS SECTION

The following annotated claims help illustrate the features defined by the claims, but are not intended to be an exhaustive listing of the claimed features. Instead, the Specification may contain many more examples of such claimed features. Thus, the following claims are not intended to be limited to or limited by the following brief annotations.

Appellants provide the following annotated claims, in which the annotations refer to the present invention's features in the text of the Specification, indicated by paragraph number and Figure number.

1. (Canceled).

2. (Previously Presented) A system for verifying integrated circuit logic of a system-on-a-chip (SOC), said system comprising:

an SOC comprising: **{[0022]-[0024]; Fig. 1, 100}**

a master central processing unit (CPU) that produces a first set of signals and a second set of signals for verifying said integrated circuit logic in

response to running a verification case; **{[0022]; Fig. 1, 130}**

an SOC interface that receives said second set of signals; **{[0022]-[0024] and [0026]; Fig. 1, 101}** and

a first external bus interface unit (EBIU) **{[0020] and[0023]; Fig. 1, 205}** that is slaved to said master CPU **{[0022]; Fig. 1, 130}** and receives said first set of signals; and

a verification test bench **{[0019], [0020], and [0022]; Fig. 1, 300}** that is external to said SOC **{[0022]-[0024]; Fig. 1, 100}**, said verification test bench **{[0019], [0020], and [0022]; Fig. 1, 300}** comprising:

a verification interface model **{[0019], [0022]-[0024], and [0026]; Fig. 1, 210)** connected to said SOC interface **{[0022]-[0024] and [0026]; Fig. 1, 101}**; and

a second EBIU **{[0019], [0020], [0022], and [0023]; Fig. 1, 200}** connected to said first EBIU **{[0020] and [0023]; Fig. 1, 205}** and to said verification interface model **{[0019], [0022], [0023], [0024], and [0026]; Fig. 1, 210}**;

wherein said first set of signals received by said second EBIU **{[0019], [0020], [0022], and [0023]; Fig. 1, 200}** is inputted to said verification

interface model **{[0019], [0022]-[0024], and [0026]; Fig. 1, 210}** and said verification interface model outputs data for said verification case to said SOC interface **{[0022]-[0024], and [0026]; Fig. 1, 101}**; and

wherein said verification case checks for correctness of said outputted data from said verification interface model **{[0019], [0022]-[0024], and [0026]; Fig. 1, 210}** to said SOC interface **{[0022]-[0024], and [0026]; Fig. 1, 101}** by said second set of signals and records a verification case status.

3-7. (Canceled).

8. (Previously Presented) A system for verifying integrated circuit logic of a system-on-a-chip (SOC), said system comprising:

an SOC comprising: **{[0022]-[0024]; Fig. 1, 100}**

a master central processing unit (CPU) that produces a first set of signals and a second set of signals for verifying said integrated circuit logic in response to signals produced by running a verification case; **{[0022]; Fig. 1, 130}**

an SOC interface **{[0022]-[0024], and [0026]; Fig. 1, 101}** that receives said second set of signals, said SOC interface being connected to said

master CPU **{[0022]; Fig. 1, 130}** by a first internal bus; and

a first external bus interface unit (EBIU) **{[0020], [0023]; Fig. 1, 205}** that is slaved and connected to said master CPU **{[0022]; Fig. 1, 130}** by a second internal bus **{[0022]; Fig. 1, 131}**; and

a verification test bench **{[0019], [0020], and [0022]; Fig. 1, 300}** that is external to said SOC **{[0022]-[0024]; Fig. 1, 100}**, said verification test bench comprising:

a verification interface model **{[0019], [0022]-[0024], and [0026]; Fig. 1, 210}** connected to said SOC interface **{[0022]-[0024], and [0026]; Fig. 1, 101}** by a second external bus **{Fig. 1, DATA}**; and

a second EBIU **{[0019], [0020], [0022], and [0023]; Fig. 1, 200}** connected to said first EBIU **{[0020], [0023]; Fig. 1, 205}** by a first external bus **{Fig. 1, 206}** and to said verification interface model **{[0019], [0022]-[0024], and [0026]; Fig. 1, 210}** by a third internal bus **{Fig. 1, 201}**;

wherein said first set of signals received by said second EBIU **{[0019], [0020], [0022], and [0023]; Fig. 1, 200}** is inputted to said verification interface model **{[0019], [0022]-[0024], and [0026]; Fig. 1, 210}** via said third internal bus **{Fig. 1, 201}** and said verification interface model outputs data for said

verification case to said SOC interface **{[0022]-[0024], and [0026]; Fig. 1, 101}** via said data bus **{Fig.1, DATA}**; and

wherein said verification case checks for correctness of said outputted data from said verification interface model **{[0019], [0022]-[0024], and [0026]; Fig. 1, 210}** to said SOC interface **{[0022]-[0024], and [0026]; Fig. 1, 101}** by said second set of signals via said first internal bus and records a verification case status.

9. (Previously Presented) The system in claim 8, wherein said verification case comprises software drivers. **{[0021]}**

10. (Previously Presented) The system in claim 8, wherein registers of said SOC interface and said verification interface model are controlled by the same verification case. **{[0022]}**

11. (Previously Presented) The system in claim 10, wherein said verification case utilizes the same software driver to configure and control said SOC interface and said verification interface model. **{[0011] and [0024]}**

12. (Previously Presented) The system in claim 10, wherein said verification case utilizes different software drivers to configure and control said SOC interface and said verification interface model. **{[0011] and [0024]}**

13. (Previously Presented) The system in claim 8, wherein said verification interface model tests an operational capability of said SOC interface. **{[0022]}**

14. (Previously Presented) The system in claim 8, further comprising an additional verification interface model for said verification test bench, said additional verification interface model being connected to said second EBIU for testing additional types of SOC interfaces. **{[0021]}**

15. (Previously Presented) A system for verifying integrated circuit logic of a system-on-a-chip (SOC), said system comprising:

an SOC comprising: **{[0022]-[0024]; Fig. 1, 100}**

a master central processing unit (CPU) that produces a first set of signals and a second set of signals for verifying said integrated circuit logic in response to signals produced by running a verification case **{[0022]; Fig. 1, 130}**;

an SOC interface **{[0022]-[0024], and [0026]; Fig. 1, 101}** that receives said second set of signals, said SOC interface being connected to said master CPU **{[0022]; Fig. 1, 130}** by a first internal bus; and

a first external bus interface unit (EBIU) **{[0020], [0023]; Fig. 1, 205}** that is slaved and connected to said master CPU **{[0022]; Fig. 1, 130}** by a second internal bus **{[0022]; Fig. 1, 131}**; and

a verification test bench **{[0019], [0020], and [0022]; Fig. 1, 300}** that is external to said SOC **{[0022]-[0024]; Fig. 1, 100}**, said verification test bench comprising:

a verification interface model **{[0019], [0022]-[0024], and [0026]; Fig. 1, 210}** connected to said SOC interface **{[0022]-[0024], and [0026]; Fig. 1, 101}** by a second external bus **{[0022]; Fig. 1, 131}**; and

a second EBIU **{[0019], [0020], [0022], and [0023]; Fig. 1, 200}** connected to said first EBIU **{[0020], [0023]; Fig. 1, 205}** by a first external bus **{Fig. 1, 101}**and to said verification interface model by a third internal bus **{Fig. 1, 201}**;

wherein said second EBIU **{[0019], [0020], [0022], and [0023]; Fig. 1, 200}** and said first EBIU **{[0020], [0023]; Fig. 1, 205}** are mastered by said

master CPU **{[0022]; Fig. 1, 130}** of said SOC, such that, said SOC interface **{[0022]-[0024], and [0026]; Fig. 1, 101}** and said verification interface model **{[0019], [0022]-[0024], and [0026]; Fig. 1, 210}** receive said first set of signals and said second set of signals, respectively, as inputs based on the running of said verification case by said master CPU; and

wherein said verification case checks for correctness of outputted data from said verification interface model **{[0019], [0022]-[0024], and [0026]; Fig. 1, 210}** to said SOC interface **{[0022]-[0024], and [0026]; Fig. 1, 101}** by said second set of signals and records a verification status.

16. (Previously Presented) The system in claim 15, wherein said verification case comprises software drivers. **{[0021]}**

17. (Previously Presented) The system in claim 15, wherein said verification case utilizes the same software driver to configure and control said SOC interface and said verification interface model. **{[0011] and [0024]}**

18. (Previously Presented) The system in claim 15, wherein verification test case

utilizes different software drivers to configure and control said SOC interface and said verification interface model. **{[0011] and [0024]}**

19. (Previously Presented) The system in claim 15, wherein said verification interface model tests an operational capability of said SOC interface.

20. (Previously Presented) The system in claim 15, further comprising an additional verification interface model for said verification test bench, said additional verification interface model being connected to said second EBIU for testing additional types of SOC interfaces. **{[0022]}**

21. (Previously Presented) A method for verifying integrated circuit logic of a system-on-a-chip (SOC), said method comprising:

producing a first set of signals and a second set of signals by a master central processing unit (CPU) **{[0022]; Fig. 1, 130}** of an SOC **{[0022]-[0024]; Fig. 1, 100}**, which includes said integrated circuit logic, in response to running a verification case on said master CPU;

slaving an SOC interface **{[0022]-[0024], and [0026]; Fig. 1, 101}**, which

receives said second set of signals, and a first external bus interface unit (EBIU) **{[0020], [0023]; Fig. 1, 205}** of said SOC **{[0022]-[0024]; Fig. 1, 100}**, which receives said first set of signals, to said master CPU of said SOC;

connecting said SOC interface **{[0022]-[0024], and [0026]; Fig. 1, 101}** to an external verification interface model **{[0019], [0022]-[0024], and [0026]; Fig. 1, 210}**, which is external to said SOC;

connecting said first EBIU **{[0020], [0023]; Fig. 1, 205}** to a second EBIU **{[0019], [0020], [0022], and [0023]; Fig. 1, 200}**, which is external to said SOC, said second EBIU being connected to said external verification interface model **{[0019], [0022]-[0024], and [0026]; Fig. 1, 210}**;

inputting said first set of signals, received by said second EBIU **{[0019], [0020], [0022], and [0023]; Fig. 1, 200}**, into said verification interface model **{[0019], [0022]-[0024], and [0026]; Fig. 1, 210}**;

inputting said second set of signals, received by said SOC interface **{[0022]-[0024], and [0026]; Fig. 1, 101}**; and

verifying said verification case by checking for correctness of said outputted data from said verification interface model **{[0019], [0022]-[0024], and [0026]; Fig. 1, 210}** to said SOC interface **{[0022]-[0024], and [0026]; Fig. 1, 101}** by said

second set of signals and recording a verification case status.

22. (Previously Presented) The method in claim 21, wherein said verification case comprises software drivers. **{[0021]}**

23. (Previously Presented) The method in claim 21, further comprising controlling registers of said SOC interface and said verification interface model by the running of the verification case on the master CPU. **{[0022]}**

24. (Previously Presented) The method in claim 23, wherein said verification case utilizes the same software driver to configure and control said SOC interface and said verification interface model. **{[0011] and [0024]}**

25. (Previously Presented) The method in claim 23, wherein said verification case utilizes different software drivers to configure and control said SOC interface and said verification interface model. **{[0011] and [0024]}**

26. (Previously Presented) The method in claim 21, further comprising

comparing said first set of signals, received by said second EBIU, and inputted into said verification interface model and said second set of signals, received from said SOC interface, and inputted into said verification interface model to test an operational capability of said SOC interface. **{[0019]-[0024] and [0026]}**

27. (Previously Presented) The method in claim 21, further comprising:

connecting at least one additional verification interface model to said second EBIU; and

testing additional types of SOC interfaces **{{[0021]}.**

28-34. (Canceled).

APPENDIX

MEANS OR STEP PLUS FUNCTION ANALYSIS SECTION

Not applicable.

APPENDIX

EVIDENCE SECTION

Not applicable.

APPENDIX

RELATED CASES SECTION

Not applicable.